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Technical report on approaches for sub-array beamformer

Work Package 3 – Design Finalization for Critical Subsystems
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Abstract

This report presents the technical requirements for implementing the EISCAT_3D test sub-array beamformer and also, evaluates the commercial beamformer approaches by considering the architectural, interconnectivity, power, bandwidth and cost requirements. The evaluated approaches are categorized as the off-the-shelf and the customized solutions. The evaluated off-the-shelf approaches are: Astron's Uniboard[1] beamformer, Siru Innovation Oy's SDR10 receiver, National Instrument's USRP RIO and FlexRIO systems. The evaluation result, of the off-the-shelf approaches, suggest that it is costly, power in-efficient and complex to implement them for the sub-array beamforming. Hence, a customized solution is required for the sub-array beamforming. As a result, this report also evaluated the customized approaches based on the vendor interactions and proposals. The evaluated customized approaches are: Astron's Uniboard[2] beamformer, National Instrument's customized system and Siru Innovation Oy's customized solution. The evaluation result of the customized approaches suggest that all these solutions will be developed by considering the sub-array beamformer requirements and further, these solutions are easy to implement than the off-the-shelf approaches. The comparison of these customized approaches suggest that all of them can accommodate 182 channels in a single system and hence, the best customized solution can be chosen based on the lowest cost, lowest power consumption and the minimum lead time. Based on our vendor interactions, it is found that the research and development (R&D) cost, to develop a customized solution, is high for single sub-array. Hence, small vendors may consider too expensive to develop a customized solution for single sub-array.

Introduction

A beamformer performs summation of signals either using analog hardware or digital computing techniques. In a large aperture array radar (LAAR) system, such as EISCAT_3D, a digital beamformer (DBF) acts as a multi-channel digital receiver that can be used to implement a large radio antenna by digitally combining the received signals on each of the individual array antennas. The use of a DBF allows more flexible polarization diversity, high system dynamic range, beam shaping, synthesis of multiple simultaneous beams and antenna beam pointing in many directions simultaneously. Further, a DBF can extract much more information in remote sensing applications than a simple analog beamformer (ABF).

Beamforming is done to precisely align the phases of the incoming signals from different array antennas in order to form a beam in specific direction. In a LAAR system, there is a physical geometric delay on the incoming wave front and it increases linearly across the array. This delay need to be compensated before being summed and it can be done in a straightforward manner by using a true time-delay ABF but it is a relatively bulky and expensive solution. So, the alternative approach would be to use either a time-delay or a phase shift DBF [1].

In a time-delay DBF, after digitizing the signal at the sub-array level, it is very simple to introduce

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delays which are a multiple of the sample time and simply buffer the signals from elements which need a delay. This DBF approach works perfectly over a wide frequency bandwidth if the signals have long time delays across the array. The main drawback with this approach is that the maximum delay length is decided by the size of the array rather than by the carrier wavelength and hence, more hardware required for implementation.

In a phase shift DBF, the signal from each antenna is delayed upto one period, 2π, to match the phase of all elements before adding up all the signals. This approach can be implemented with less cost and hardware compared to time-delay DBF. However, this approach is applicable only to narrowband situations where the incoming wave is coherent over the entire array. As the incoming waves are both wideband (~ 30 MHz) and change faster than the size of the array, phase shift DBF is not applicable for test sub-array beamforming. Hence, time-delay DBF approach should be used in the EISCAT_3D test sub-array system [2].

DBFs can be realized using either field programmable gate arrays (FPGAs) or cluster computers. The real time processing of the signal for EISCAT_3D system exhibits highly parallel characteristics and hence, the hardware platforms, for realizing the DBF, requires parallel processors such as FPGAs. The FPGAs have greater bandwidth capability and sufficiently high input-output rate compared to cluster computers. Further, FPGAs have a long operational life and are highly power efficient compared to computers. However, the per unit cost of a computer may be less than the per unit FPGA cost but the overall FPGA based implementation cost will be less than the cluster computer based solution as the total number of FPGA units required will be less than the computer units due to the recent advances in semiconductor technology. The above mentioned benefits suggests that it is more practical to realize EISCAT_3D test sub-array DBF using FPGA technology.

Description of EISCAT_3D Test Sub-Array

During EISCAT3D_PfP project, a EISCAT_3D test sub-array system will be produced and tested at EISCAT's Ramfjordmoen facility in Norway. This demonstrator will be similar to the final sub-array configuration that will be deployed at the core site in future. The total size of this test sub-array will be approximately 10m x 10m, with an additional buffer for safety reasons. This test sub-array will transmit a total peak output power of 100 kW (500W per polarization) in the frequency band of 227-239 MHz with center frequency around 233 MHz and minimum bandwidth of 5 MHz. The receiver frequency band is 218-248 MHz with center frequency around 233 MHz and analog bandwidth of 30 MHz. A top level block diagram of the different subsystems in the test sub-array is shown in Figure 1.

The test sub-array system consists of following sub-systems:

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1) Radar sub-array unit, made up of 91 inverted v-shaped crossed dipole antenna elements, mounted approximately 2m above the ground on a meshed metallic support structure.
2) RF front end unit is made up of low noise amplifier (LNA) and anti-aliasing filter.
3) Sub-array beamformer unit consists of analog to digital converters (ADC) and a digital beamformer.
4) The transmit unit consists of a power amplifier, transmit/receive switch and a power supply unit.
5) Pulse and steering unit consists of a radar controller unit, an exciter, and an interface.
6) Status and control unit is made up of input/output serial and parallel ports connected to a computer.
7) Time and frequency unit consists of a white rabbit master and slave sub-unit, time and frequency synchronisation sub-unit and clock generator sub-unit.
8) Computing system is a computer to store and process the measurement data.

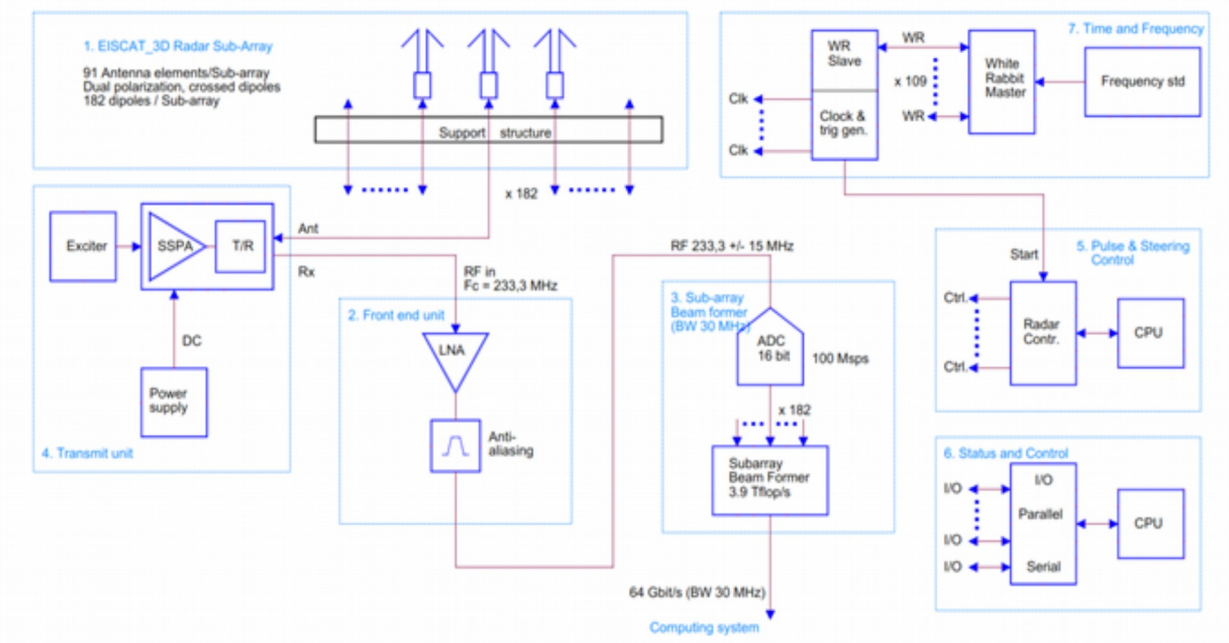

Figure 1: A top level block diagram of the different subsystems in the EISCAT_3D test sub-array.

Sub-Array Beamformer Requirements

The sub-array beamformer sub-system consists of 14 or 16 bit ADCs and a DBF. The DBF must be able to handle 10 simultaneous beams over the full bandwidth. The network and capacity requirements of this sub-system/test sub-array are calculated with the support of the Nordic e-Infrastructure Collaboration (NeIC) project [3]. The summary of the technical requirements of ADC and DBF are presented in Table 1 and Table 2, respectively. The top level block diagram of the DBF

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along with the interfaces is shown in Figure 2. The sub-array beamformer interfaces can be listed as follows:

- Antenna Signals (RFin Ant. Apol & RFin Ant. Bpol): The analog antenna signals (182) which are sufficiently amplified and filtered to drive ADCs from the individual crossed v-dipole antennas. The RF input signals, RFin Ant. Apol. and RFin Ant. Bpol., are different in polarization and hence, can be processed independently in the beamformer.
- ADC output signals (Data Ant. Apol & Data Ant. Bpol): The 16 bit (15 bit data and 1 bit sync) ADC output signal is the digital input to the sub-array beamformer at a sampling rate of 100 Msps.
- Beams: The 10 simultaneous beams per polarization resulting out of the sub-array beamformer are the voltage sums of the individual antennas and they are together represented as single arrow.

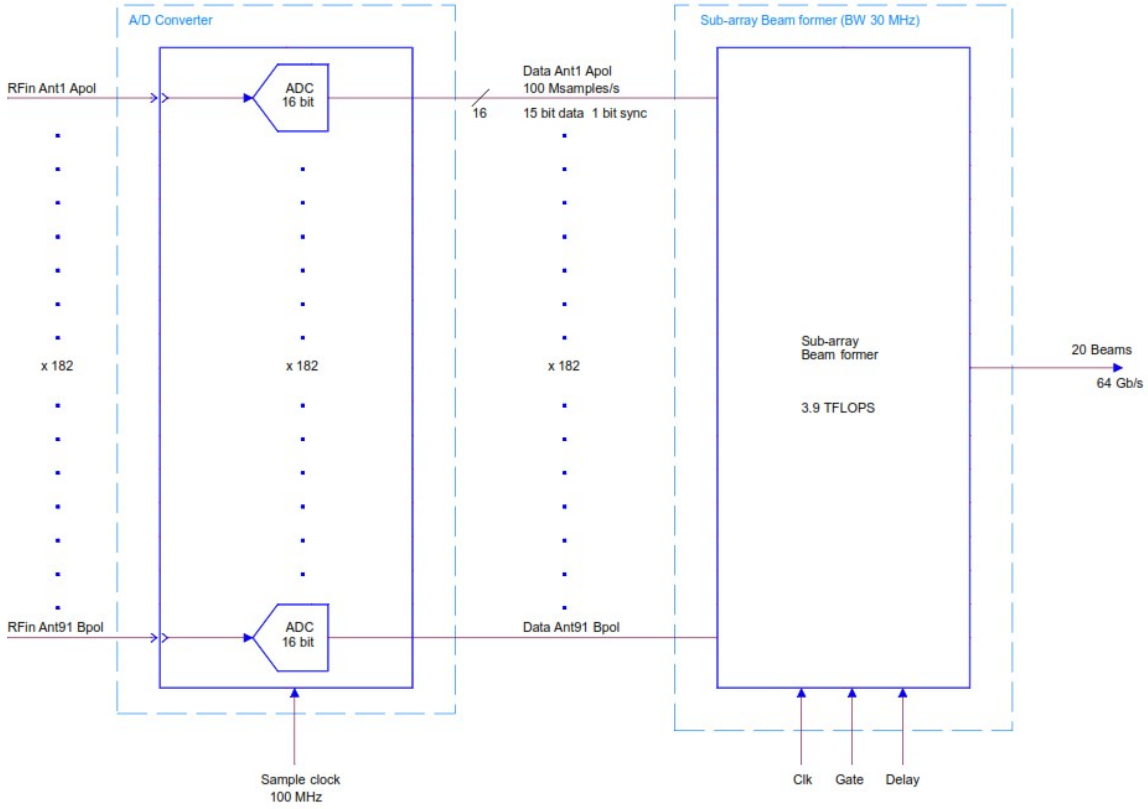

Figure 2: The Block diagram of EISCAT_3D sub-array beamformer.

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Table 1: ADC technical requirements.

Parameter	**Value**
Center Frequency	233 MHz
Bandwidth, analog	30 MHz
Sampling Rate	100 Msps
ADC resolution	14- or 16-bit
ADC timing error	< 120 ps
Signal to Noise ratio (SNR)	> 70 dB
Spurious free dynamic range (SFDR)	(SNR+10) dB

Table 2: DBF technical requirements.

Parameter	**Value#1**
Number of Antennas	91
Number of polarizations	2
Sample rate	100 MHz
Bandwidth	30 MHz
Filter type & length	36-tap (real coefficient) DSP-FIR filter
Filter Resolution	18 bits
Group & phase delay error combined	≤ 5.8 ps
Multiplications and Additions (MACs) per filter	36
Computing requirement per sub-array for 10 simultaneous beams	3.9 TFLOPS
Network requirement per sub-array	64 Gbit/s
Signal to Noise ratio (SNR)	> 70 dB

- Clock: The clock signal is for the digital processing of the beamformer data.

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- Controls: Gate and delay signals are used as control signals for the sub-array beamformer operations.

Capacity requirements

The beam forming performed in the sub-array is essentially a series of digital signal processing (DSP) operations. The lower bound on computing power for these DSP operations in the test sub-array can be calculated. Each data stream coming from a single polarization of an antenna is sampled digitally at 100 MHz [4], resulting in 30 MHz of complex in-phase and quadrature samples. These are passed through a 36 tap (real coefficient) DSP Finite Impulse Response (FIR) filter with delays in the order of picoseconds applied [2]. The number of Multiplications and Additions (MACs) required per FIR filter is generally one. Hence, the total number of MACs required for each FIR filter are 36.

Computing power is generally expressed in Floating-point Operations Per Second (FLOPS) and it is calculated using the bandwidth and the number of MACs per FIR filter as follows:

$$30 \times 10^6\,\mathrm{s}^{-1} \times 36\ \mathrm{MAC} = 1.08 \times 10^9\,\mathrm{MAC/s}$$

Usually 1 floating-point MAC is considered equivalent to 2 floating-point operations and therefore

$$1.08 \times 10^9\,\mathrm{MAC/s} \times 2\ \mathrm{FLOP/MAC} = 2.16 \times 10^9\ \mathrm{FLOPS}$$

per data stream.

At the sub-array level, the 182 data streams (91 antennas each with 2 polarizations) are formed into 10 wide-angle beams. This results in a total sub-array computing requirement of 2.16 GFLOPS× 182×10 = **3.93 TFLOPS**. A consideration must be made that at the sub-array level the output data must be screened for satellite trajectories. This will require input from the EISCAT_3D operations centre computing to sub-array computing and will require some more computing capacity.

Network requirements

The network for the test sub-array computing must receive the data streams from the antennas via the analog to digital converters (ADCs). The signals from the ADCs must be passed by network cables to the back plane or bus of the DSP computing described above. After the beams are formed, the output data must be passed by the network back to the Ramfjordmoen controlling station.

The data rate that arrives at the sub-array computing from each dipole antenna is as follows:

- The analogue signal is passed through a band pass filter, with bandwidth of 30 MHz.

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- Hence, each polarization direction is sampled at an optimal rate of 100 MHz due to under-sampling of signals [4].

- An ADC converts each sample to a 16 bit digital signal.

This results in a digital bit-rate per dipole of each antenna of:

$$16 \text{ bits} \times 100 \times 10^6 \text{ s}^{-1} \approx 1.6 \text{ Gbit/s}$$

Hence, the test sub-array infrastructure will need a connection between each ADC (182 per sub-array) and input of the DSP computing of at least 1.6 Gbit/s. The signal at this stage is a series of 16 bit numbers (with one bit reserved for timing to be discussed) arriving at a rate of 100 MHz.

As described above, the 10 wide-angle beams are formed in the sub-array DSP processing. In order to avoid round-off errors [5] the data from the wide-angle beams are stored as 32 bit numbers (with precise timing information incorporated). Hence, the total anticipated data rate from a sub-array with EISCAT_3D operating at 30 MHz bandwidth is

$$10 \times 2 \times 32 \text{ bit} \times 100 \times 10^6 \text{ s}^{-1} \approx \mathbf{64 \text{ Gbit/s}}$$

If it is necessary to transmit data back to the Ramfjordmoen controlling station then the test sub-array must have a wide-area connection that can handle approximately 64 Gbit/s.

Sub-Array Beamformer Approaches

The sub-array beamformer approaches can be mainly categorised as the off-the-shelf and the customized approaches. The currently available off-the-shelf solutions are Uniboard[1] approach from Astron, Netherlands, Software defined radio approach, SDR10 device, from Siru Innovations Oy and National Instrument's USRPRIO and FlexRIO solutions. The customized solutions are from same vendors but tailored according to the needs of EISCAT_3D test sub-array beamformer.

The off-the-shelf and customized approaches are evaluated by considering the architectural, interconnectivity, power, bandwidth and cost requirements of EISCAT_3D test sub-array beamformer.

Off-the-shelf Approaches

Uniboard[1] Approach

The Uniboard is a universal high performance processing board that uses FPGA firmware based

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technology and is made up of 14 layers. The initial version of Uniboard (Uniboard[1]) consists of 8 FPGAs, interconnected by a high speed transceiver mesh, integrated in one board with a processing capability of 2 TMAC/s. The Uniboard has standard plane interfaces and can be used as a stand-alone processing board. A hardware layout of the Uniboard[1] is shown in Figure 3 [6]. The Uniboard[1] technology is applied for beamformer and correlator in APERTIF [7], JIVE correlators, radio frequency interference (RFI) mitigation, digital receivers and pulsar binning machine. For a larger system application, multiple Uniboard[1]s have to be combined and thus, result in more power consumption and also, increase in FPGA board temperature. The FPGA board temperature can be reduced by using the water cooling technique whereas the power consumption can be reduced by using Uniboard[2] processing board with more input channels than Uniboard[1] and thus, reducing the number of boards required for implementing a large system.

Uniboard[1] Beamformer for EISCAT test sub-array:

The 91 dual polarized antennas in a test sub-array must be combined, using 16 input channel Uniboard[1] beamformer, to form 10 simultaneous beams for each polarization and it must be ensured that both polarizations are processed independently of each other. Assuming 16 bits digitization with a sample rate of 100 MHz and 30 MHz bandwidth, a total of 16 channels can be connected to one Uniboard[1]. Hence, for a test sub-array with 91 dual polarized antennas (91*2 channels) total of 6 Uniboard[1] processing boards per polarization are needed for interconnections where as for the purpose of processing only one board is sufficient. With 6 Uniboard[1]s per sub-rack, total of 2 sub-racks are needed for two polarizations. Multiple sub-racks are interconnected through 10 Gb Ethernet connections and beamforming is done on the front nodes (FNs) as shown in Figure 3. Each FN will calculate all the beams for a subset of sub-bands. This implies that the sub-bands need to be distributed over the board, backplane and sub-racks. On the board itself this is done through the high speed mesh, within one sub-rack all back nodes (BNs) 0 (through 3) of all boards are interconnected, and finally all sub-racks are connected by interconnecting boards 0 (through 5) of each sub-rack.

General considerations, power consumption, price of Uniboard[1]:

The Uniboard[1] beamforming solution can be implemented using easily available hardware and it is being used in APERTIF [7]. Some of the main features of this technology are:

- Availability of ready-made firmware specifically written for Uniboard
- Standard interfaces
- Linear scaling with bandwidth
- Same type of hardware needed to produce and maintain (FPGAs with identical footprints)

The Uniboard[1] has power consumption of 400 W per board when subjected to maximum load but on an average it consumes 350 W. With a total of 12 boards for EISCAT_3D test sub-array, the total power (average) consumed will be 4.2 kW per sub-array and it will be 458 kW for EISCAT_3D

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array (109 sub-arrays). The power consumption associated with the cooling of FPGAs will be around 30%, leading to a total power consumption of 5.5 kW per sub-array. If we assume that around 40 W of power consumed by A/D units then the total power consumption per sub-array will be approximately 5.9 kW.

The price of the Uniboard[1] is about 15 kEuro per board, in a production of only nine boards. At this price, the 12 boards needed for test sub-array will cost 180 k Euro and the total price of A/D units

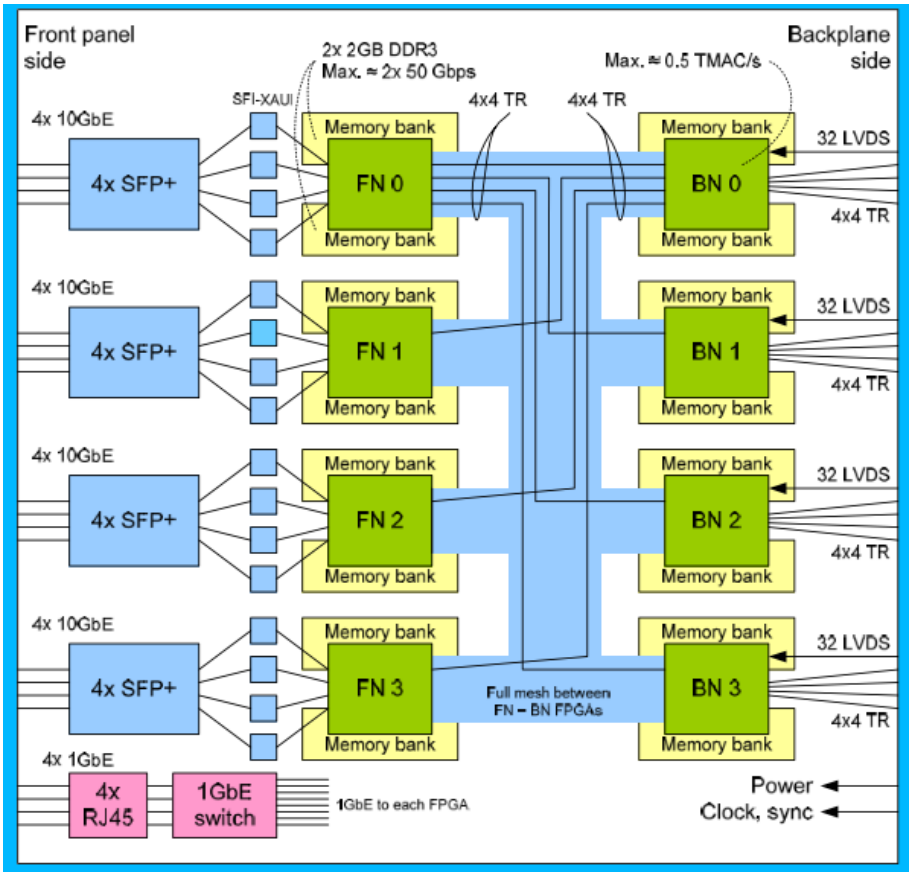

Figure 3: Uniboard[1] hardware, taken from [6].

will be approximately 1.5 kEuro. Hence, the total price for implementing Uniborad[1] beamformer for the test sub-array is 181.5 kEuro. In bulk this price should go down considerably, to an estimated 10 kEuro/Uniboard[1] and thus, the total price will be much less if this Uniboard beamforming technology is used for EISCAT_3D array. Considering the features of this technology, price, size and power consumption budget the Uniboard[1] is a good beamforming solution for EISCAT_3D test sub-array but it is always good to have a power efficient Uniboard with more input channels and thus, resulting in less number of processing boards.

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Software Defined Radio Approaches

A software defined radio (SDR) is a radio communication system where the components are implemented using software on a computer or an embedded system. SDRs are considered as a possible prototyping option for the next generation technology by allowing quick prototyping a system, characterizing the performance and iteration of design. SDR based beamforming solutions for EISCAT_3D system have been discussed in [4, 8] and further, it is suggested, in [4], that daisy-chained topology is better compared to star topology for implementing SDR based beamforming solution. The commercially available SDR-based digital receivers, used for beamforming, are SDR10 device from Siru Innovation, USRP Rio and FlexRio from National Instruments (NI).

Siru SDR10 System for test sub-array

Siru Innovation Oy's SDR10 [9] is a high performance scalable software defined radio platform for designing and deploying next generation systems. A block diagram of SDR10 device is shown in Figure 4. It is an 8-channel digital receiver capable of performing beamforming for EISCAT_3D test sub-array. Assuming 16 bits digitization with a sample rate of 100 MHz and 30 MHz bandwidth, the beamforming is performed by combining the 91 dual polarized antenna signals using 24 SDR10 daisy chained receivers and thus, resulting in 10 simultaneous beams for each polarization. The average power consumed by each SDR10 receiver is 7 W and hence, the total power consumed by 24 receivers is 168 W. The price of each SDR10 receiver is around 4 kEuro and the total price for implementing the test sub-array is 96 kEuro. The SDR10 receiver is power efficient compared to Uniboard[2] approach but approximately 3 times more expensive. Also, implementing the SDR10 receiver solution using daisy chain topology requires more cables and a lot of space for mounting 24 SDR10 receivers.

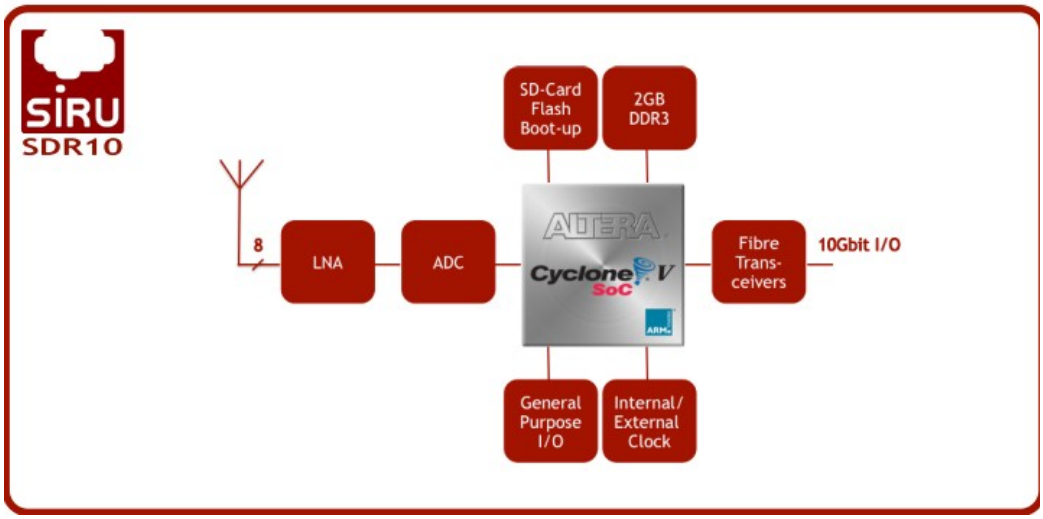

Figure 4: Block diagram of SDR 10, taken from [9].

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NI USRP RIO System for test sub-array

The Universal Software Radio Peripheral (USRP) reconfigurable input-output (RIO) system from National Instruments (NI) is a software defined radio platform [10]. The USRP Rio combines 2 full duplex transmit and receive channels with 40 MHz/channel of real time bandwidth and a large digital signal processing (DSP) oriented Kintex7 FPGA. This FPGA acts as interface to the analog RF front-end as shown in Figure 5. USRP Rio System has been considered for beamforming of EISCAT_3D system during preparatory phase and detailed description is found in [4, 8]. Also, 64 USRP RIO units are stacked together for beamforming in Massive MIMO testbed with 128 channels and details are found in [11]. Assuming 16 bits digitization with a sample rate of 100 MHz and 30 MHz bandwidth, the test sub-array beamforming is performed by combining the 91 dual polarized antenna signals using 92 daisy chained USRP RIO SDRs and thus, resulting in 10 simultaneous beams for each polarization. The average power consumed by each USRP RIO SDR is approximately 41 W and hence, the total power consumption for 92 units is approximately 3.8 kW. The price of each USRP RIO SDR is approximately 6.8 kEuro and hence, the total price required to implement test sub-array beamforming is 625.6 kEuro. The USRP RIO SDR is very expensive and less power efficient compared to Uniboard^2 and Siru's SDR system.

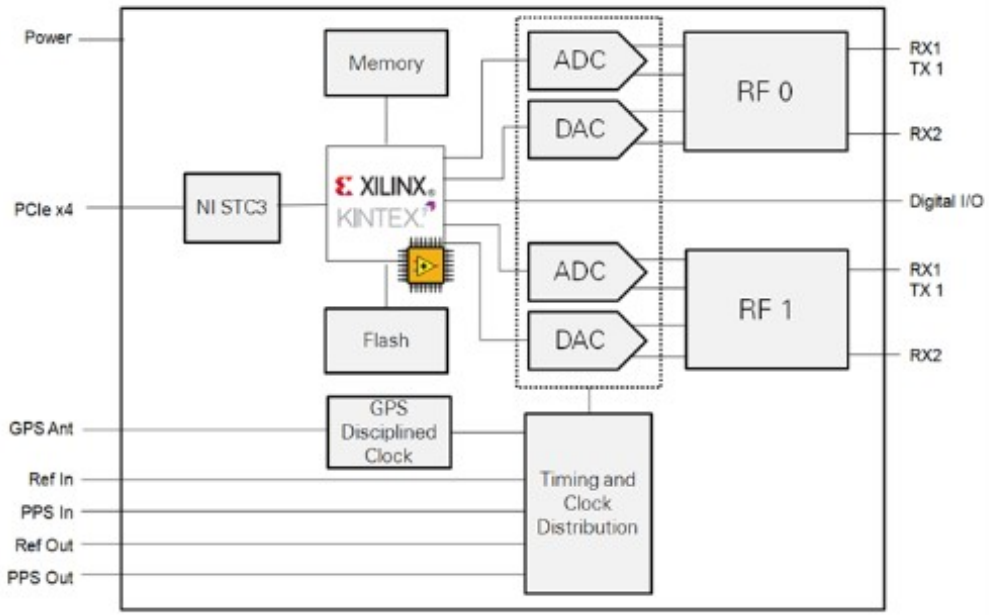

Figure 5: Block diagram of USRP Rio System, taken from [10].

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NI FlexRIO System for test sub-array

The National instruments FlexRIO is a modular system providing integrated hardware and software for rapid prototyping of next generation systems. The hardware in FlexRIO system consists of NI manufactured FPGA boards and front-end units whereas the software is NI LabVIEW system design software. The FPGA motherboard connects to the backplane of a high speed, low latency PXI Express bus, which is connected to a control computer with LabVIEW software. The applications of FlexRIO system are 8×8 MIMO system, synchronization of heterogeneous networks, LTE relaying, RF compressive sampling, spectrum sensing, cognitive radio, beamforming, and direction finding. Further, it is used in developing the first real-time 3D optical coherence tomography [12] in the world. Assuming that an 8 input channel FlexRIO system is used for EISCAT_3D test sub-array beamforming then the total number of FlexRIO units required to implement test sub-array beamforming are 24 for both polarizations and these FlexRIO units can be connected together using daisy chain topology. The power consumed per FlexRIO unit depends on contents of the adapter module and the LabVIEW reconfigured FPGA for specific application. However, assuming that the power consumed by each FlexRIO is 36 W, the total power consumption for test sub-array beamformer will be approximately 0.86 kW. The price of each FlexRIO unit is approximately 52 kEuro and the total price for 24 units is 1248 kEuro. The FlexRIO system is very expensive compared to solutions that are discussed in this report and hence, it cannot be considered as a possible solution for test sub-array beamformer.

Customized Approaches

Uniboard^2 Beamformer

The Uniboard^2 is a universal processing platform that uses the same idea as that of Uniboard^1 but re-designed completely using Altera's 20nm FPGAs compatible with 14nm devices. As shown in Figure 6, the Uniboard^2 consists of 4 FPGAs, interconnected by a high speed transceiver mesh, integrated in one board with a processing capability ranging from 5-21 TMAC/s. The Uniboard^2 has standard plane interfaces and can be used as a stand-alone processing board. The UniBoard^2 utilizes 24 Quad Small Form-factor Pluggable (QSFP) links which consists of 4 lanes running at 10 Gbps on one side. For this 24 transceivers of each FPGA are used. Another 24 are used to connect the FPGAs in a ring, such that the board can be used for a beamformer application. Furthermore, 48*4 lanes are connected to a backplane interface. The backplane can be used to connect multiple boards for large system applications. The Uniboard^2 technology is currently applied for SKA LFAA beamformer and correlator and it is described in detail in [13-14]. The power efficiency of Uniboard^2 is much higher than Uniboard^1 as the requirement of number of multiple boards, for large system application, is reduced.

Uniboard^2 Beamformer for test sub-array:

The 91 dual polarized antennas in a test sub-array must be combined, using the available 192 input

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channel Uniboard^2 beamformer, to form 10 simultaneous beams for each polarization and it must be ensured that both polarizations are processed independently of each other. Assuming 16 bits digitization with a sample rate of 100 MHz and 30 MHz bandwidth, a total of 182 channels can be connected with the transceivers on the backplane side of Uniboard^2. Hence, for a test sub-array with 91 dual polarized antennas (91*2 channels), 1 Uniboard^2 is required for both polarizations. Combining the beamformer functionality for both polarizations will limit the number of UniBoard^2 to only one per sub-array. The output beams can be distributed via the links on the front-side of the board.

Since one Uniboard^2 has to be shared between the two polarizations, a customized solution is required for implementing the test sub-array beamformer on Uniboard^2. However, the backplane solution proposed in [13] can be used to some extent under the assumption that maximum four connectors can be used on one small sized A/D unit and hence, a total of 46 A/D units are needed to feed one Uniboard^2 as shown in Figure 7. The AD9656 from Analog devices Inc.,[15] is a low power and high speed ADC with JESD204B serial interface and it is compatible with Uniboard^2 for test sub-array beamforming.

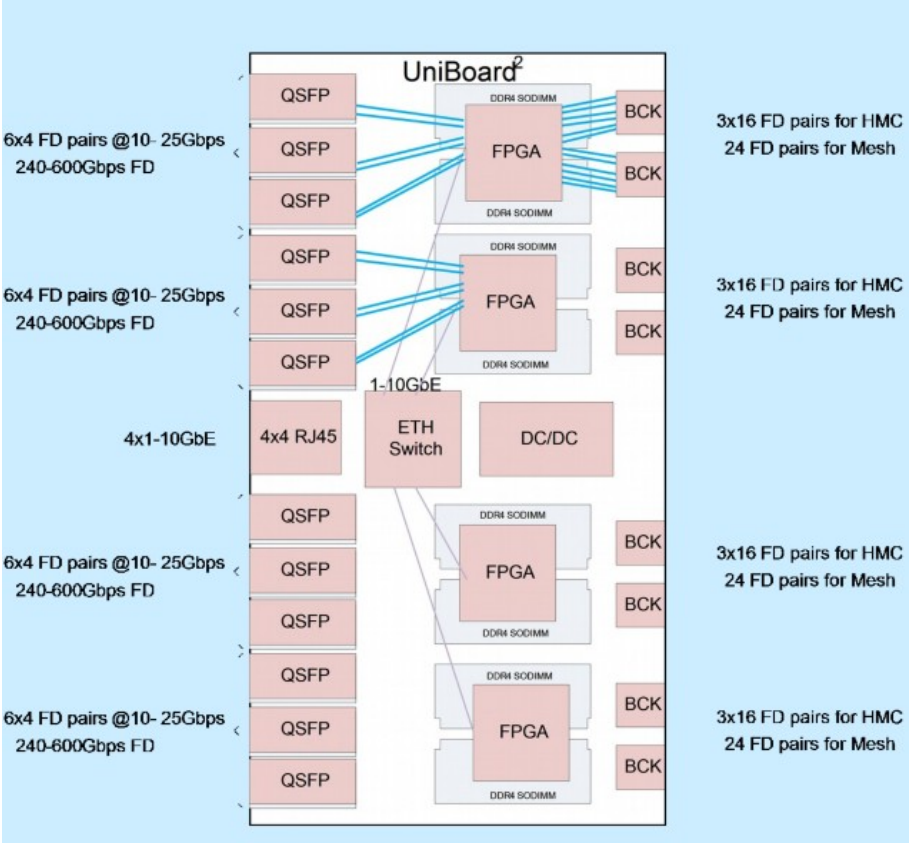

Figure 6: Uniboard^2 hardware, taken from [13].

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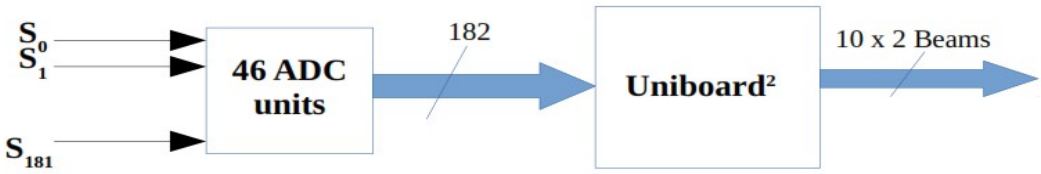

Figure 7: Customized Uniboard^2 Beamformer for test sub-array.

General considerations, power consumption and price of Uniboard^2:

The Uniboard^2 beamforming solution can be implemented using available hardware and it is being used in LFAA SKA [13]. Some of the main features of this technology are as follows:

- Availability of ready-made firmware specifically written for Uniboard^2;
- Standard interfaces with more input channels compared to Uniboard^1;
- Linear scaling with bandwidth;
- Same type of hardware needed to produce and maintain (FPGAs with identical footprints).

The Uniboard^2 has power consumption of around 500 W per board. With a total of 1 board for single EISCAT_3D sub-array, the total power consumed will be 54.5 kW for EISCAT_3D array (109 sub-arrays). The power consumption associated with the cooling of FPGAs will be around 30% of single Uniboard^2 power consumption and each A/D unit, AD 9656, consumes 0.8 W. Hence, the total power consumption per sub-array is the sum of power consumed by Uniboard^2, FPGA cooling and 46 A/D units and is found to be approximately 690 W. Thus, the total power consumption for EISCAT_3D array will be approximately 75 kW.

The price of the Uniboard^2 is about 20 kEuro per board, in a production of only nine boards and the price of each AD9656 A/D unit is around 280 Euro. Hence, the total price of Uniboard^2 and 46 A/D units will be approximately 33 kEuro. In bulk this price should go down considerably, to an estimated 25 kEuro per sub-array and thus, the total price will be much less if this Uniboard^2 beamforming technology is used for EISCAT_3D array. Uniboard^2 is a better beamforming solution for EISCAT_3D test sub-array because it has good channel density and also, efficient in terms of power and cost compared to Uniboard^1.

Customized NI System for test sub-array

National Instrument is planning to develop a new customized beamforming solution targeting EISCAT_3D test sub-array. The customized system will have 3 rack units (RU) and each RU is made up of 64 channels. Thus, the whole system will have 192 channels. Each RU is designed with modern FPGAs and these FPGAs are interconnected with each other, to combine 192 channels, for

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generating the required number of simultaneous beams per polarization. Further, a customized circuit card with RF front ends and ADCs will be part of this new system.

The 91 dual polarized antennas in a test sub-array must be combined, using the available 192 channel NI customized system, to form 10 simultaneous beams for each polarization and it must be ensured that both polarizations are processed independently of each other. Assuming 16 bits digitization with a sample rate of 100 MHz and 30 MHz bandwidth, a total of 182 channels can be connected with the 3 RU NI system as shown in Figure 8. Hence, for a test sub-array with 91 dual polarized antennas (91*2 channels), a single NI customized system is sufficient for both polarizations. Further, this system will support white rabbit synchronisation and traditional 10 MHz/PPS. Based on our calculations, the estimated average power consumption of this system will be around 0.55 kW and the total cost may range from 80 to 90 kEuro.

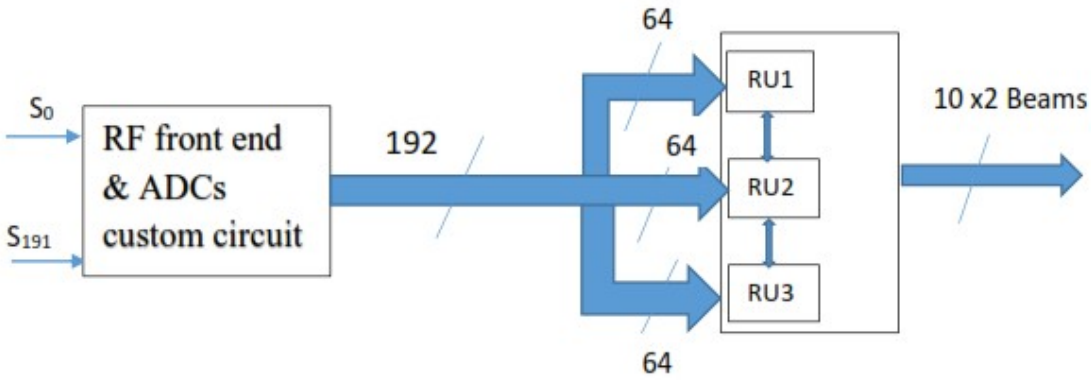

Figure 8: Customized NI System for test sub-array beamforming.

Customized Siru System for test sub-array

Siru Innovations Oy is planning to develop a customized solution for test sub-array beamforming. The customized system is a 192 channel single board test sub-array beamformer solution. This board consists of a multi-channel ADC and a modern FPGA with high processing capability. Further, this board will have modern interface to the front end unit, single clock per sub-array and also supports a 100 Gbit/s network connection. This system is expected to be a lowest power consumption solution compared to others.

Assuming 16 bits digitization with a sample rate of 100 MHz and 30 MHz bandwidth, the beamforming is performed by combining the 91 dual polarized antenna signals using a customized 192 channel single board and thus, resulting in 10 simultaneous beams for each polarization. An illustration of this customized system is shown in Figure 9. Based on our calculations, the expected total average power consumed by this customized system is 0.25 kW and the price will be around 30 kEuro.

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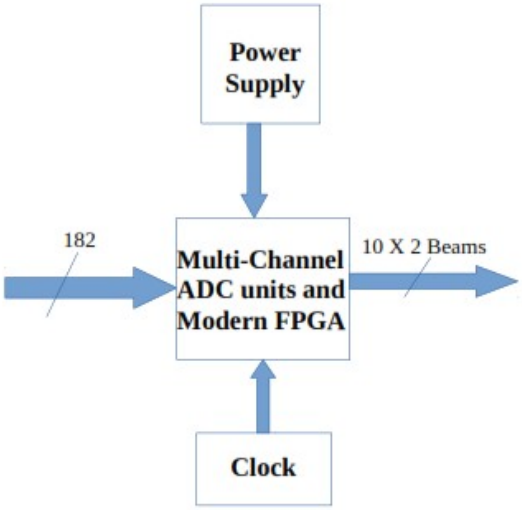

Figure 9: Customized Siru System for test sub-array beamforming.

Conclusions

A summary of the evaluated off-the-shelf approaches is presented in Table 3. The evaluation of the off-the-shelf approaches suggest that these solutions are not only complex to implement but also expensive. Although Siru's SDR 10 solution is the most power efficient, it is not suitable for test sub-array beamforming because of high cost and complexity of implementation. Hence, a customized solution is needed for test sub-array beamforming.

Table 3: Summary of off-the-shelf approaches.

Approach	Total units required	Total Power Consumption (kW)	Price (kEuro)
Uniboard[1] +ADC units	12 Uniboard[1] and 48 ADC units	5.9	181.5
Siru's SDR10	24	0.17	96
NI USRP RIO	92	3.8	625.6
NI FlexRIO	24	0.86	1248

A summary of the evaluated customized approaches is shown in Table 4. The evaluation of the customized approaches was based on the vendor interactions. The evaluation result suggest that these solutions are compact, easy to implement, easy to scale, power- and cost-efficient compared to

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the off-the-shelf approaches. All the customized approaches have the capability to accommodate 182 channels in a single unit/board/system and thus, reducing the number of cables/connectors. The comparison of customized approaches suggest that Siru's customized system is estimated to be the most power- and cost-efficient compared to other customized approaches. However, the total costs (including R&D cost) of building Siru's customized system will be much higher if Siru Innovation Oy does not use their own resources. Further, Astron and NI have previously produced beamforming system for large antenna array unlike Siru Innovation's Oy. Apart from above considerations, it must be noted that power consumption and price of NI system, shown in Table 4, include RF front end unit unlike Astron Uniboard^2. The customized NI system consumes less power compared to Astron's Uniboard^2 but it is less cost efficient. Hence, these customized approaches can best fit the EISCAT_3D sub-array beamforming if Astron can reduce the power consumption of Uniboard^2, NI can lower the cost of their system and Siru Innovation Oy can use their own resources for R&D of their system.

Table 4: Summary of customized approaches.

Approach	Total units required	Total Power Consumption (kW)	Price/unit (kEuro)
Uniboard^2+ADC units	1 Uniboard^2 and 46 ADC units	0.69	33
Siru's System	1 board including ADC units	0.25	30
NI System	1 Unit including ADC units & RF front end custom circuit	0.55	80-90

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